MC100EP809

3.3V 2:1:9 Differential HSTL/PECL/LVDS to HSTL Clock Driver with LVTTL Clock Select and Enable

ON Semiconductor®

www.onsemi.com

Description

The MC100EP809 is a low skew 2:1:9 differential clock driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The part is designed for use in low voltage applications which require a large number of outputs to drive precisely aligned low skew signals to their destination. The two clock inputs are one differential HSTL and one differential LVPECL. Both input pairs can accept LVDS levels. They are selected by the CLK_SEL pin which is LVTTL. To avoid generation of a runt clock pulse when the device is enabled/disabled, the Output Enable (OE), which is LVTTL, is synchronous ensuring the outputs will only be enabled/disabled when they are already in LOW state (Figure 9).

The MC100EP809 guarantees low output−to−output skew. The optimal design, layout, and processing minimize skew within a device and from lot to lot. The MC100EP809 output structure uses open emitter architecture and will be terminated with 50 Ω to ground instead of a standard HSTL configuration (Figure 7). To ensure the tight skew specification is realized, both sides of the differential output need to be terminated identically into 50 Ω even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

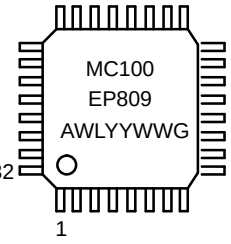
Designers can take advantage of the EP809's performance to distribute low skew clocks across the backplane of the board. Both clock inputs may be single−end driven by biasing the non−driven pin in an input pair (Figure 8).

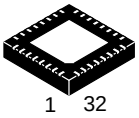
Features

- 100 ps Typical Device−to−Device Skew
- 15 ps Typical within Device Skew
- HSTL Compatible Outputs Drive 50 Ω to GND with no Offset Voltage
- Maximum Frequency > 750 MHz
- 850 ps Typical Propagation Delay
- Fully Compatible with Micrel SY89809L
- PECL and HSTL Mode Operating Range: V_{CCI} = 3 V to 3.6 V with GND = 0 V, V_{CCO} = 1.6 V to 2.0 V
- Open Input Default State
- These Devices are Pb−Free and are RoHS Compliant

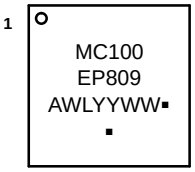
MARKING DIAGRAMS*

32−LEAD LQFP
FA SUFFIX
CASE 873A





QFN32
MN SUFFIX
CASE 488AM

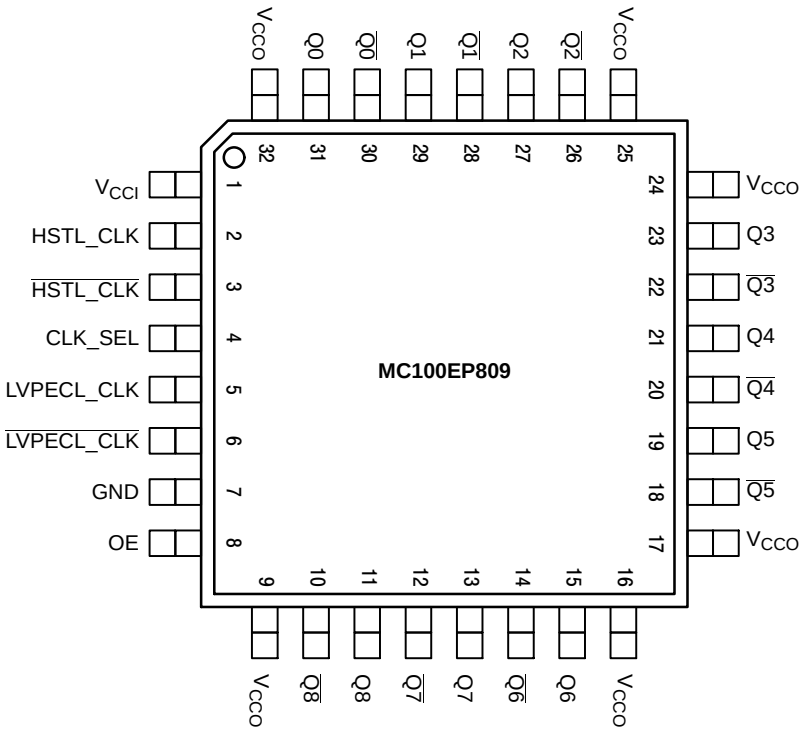


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.



All V_{CCI}, V_{CCO}, and GND pins must be externally connected to appropriate Power Supply to guarantee proper operation ($V_{CCI} \neq V_{CCO}$).

Figure 1. 32−Lead LQFP Pinout (Top View)

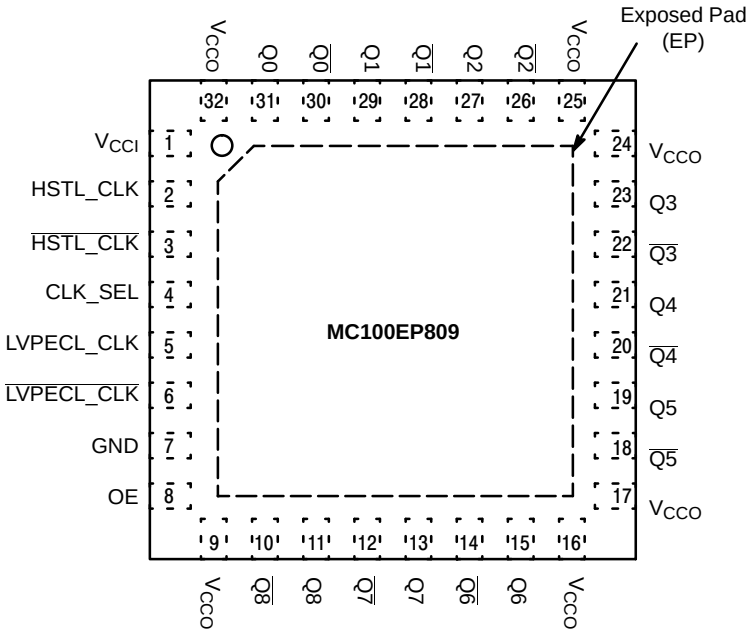


Figure 2. 32−Lead QFN Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
HSTL_CLK*, $\overline{\text{HSTL\_CLK}}$**	HSTL or LVDS Differential Inputs
LVPECL_CLK*, $\overline{\text{LVPECL\_CLK}}$**	LVPECL or LVDS Differential Inputs
CLK_SEL**	LVCMOS/LVTTL Input CLK Select
OE**	LVCMOS/LVTTL Output Enable
Q0 − Q8, $\overline{\text{Q0}}$ − $\overline{\text{Q8}}$	HSTL Differential Outputs
V_{CC1}	Positive Supply_Core (3.0 V − 3.6 V)
V_{CC0}	Positive Supply_HSTL Outputs (1.6 V − 2.0 V)
GND	Ground
EP	The exposed pad (EP) on the QFN−32 package bottom is thermally connected to the die for improved heat transfer out of the package. THe exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to GND.

* Pins will default LOW when left open.
** Pins will default HIGH when left open.

Table 2. TRUTH TABLE

OE*	CLK_SEL	Q0 − Q8	$\overline{\text{Q0 − Q8}}$
L	L	L	H
L	H	L	H
H	L	HSTL_CLK	$\overline{\text{HSTL\_CLK}}$
H	H	LVPECL_CLK	$\overline{\text{LVPECL\_CLK}}$

*The OE (Output Enable) signal is synchronized with the rising edge of the HSTL_CLK and LVOCL_CLK signals.

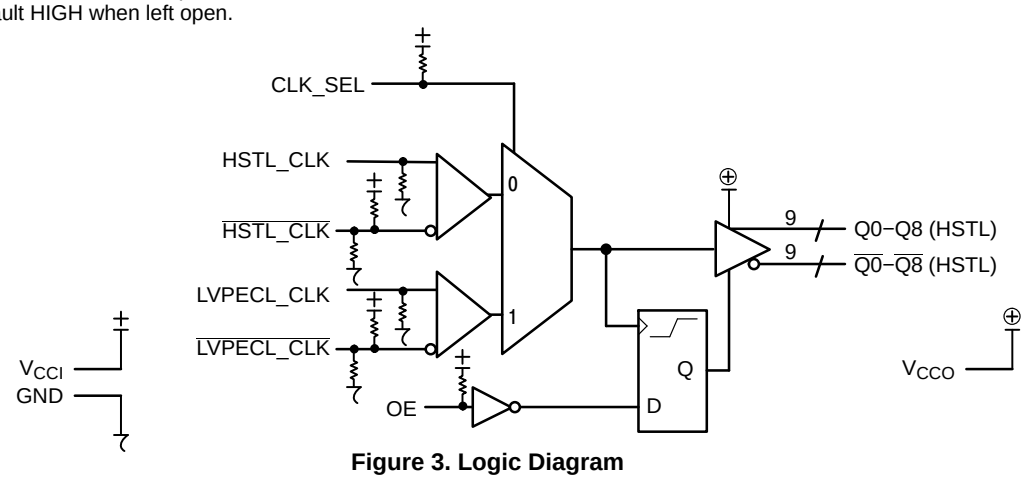


Figure 3. Logic Diagram

Table 3. ATTRIBUTES

Characteristics		Value	
Internal Input Pulldown Resistor		75 kΩ	
Internal Input Pullup Resistor		37.5 kΩ	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 2 kV	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb Pkg	Pb−Free Pkg
	LQFP−32 QFN−32	Level 2 N/A	Level 2 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
Transistor Count		478 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC1}	Core Power Supply	GND = 0 V	V_{CC0} = 1.6 to 2.0 V	4	V
V_{CC0}	HSTL Output Power Supply	GND = 0 V	V_{CC1} = 3.0 to 3.6 V	4	V
V_I	Input Voltage	GND = 0 V	$V_I \le V_{CC1}$	4	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	LQFP−32 LQFP−32	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	LQFP−32	12 to 17	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	QFN−32 QFN−32	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P	QFN−32	12	°C/W
T_{sol}	Wave Solder Pb Pb−Free			265 265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. LVPECL DC CHARACTERISTICS V_{CCI} = 3.0 V to 3.6 V; V_{CCO} = 1.6 V to 2.0 V, GND = 0 V

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	Core Power Supply Current	75	95	115	75	95	115	75	95	115	mA
V_{IH}	Input HIGH Voltage (Single−Ended)	V_{CCI} − 1.165		V_{CCI} − 0.88	V_{CCI} − 1.165		V_{CCI} − 0.88	V_{CCI} − 1.165		V_{CCI} − 0.88	V
V_{IL}	Input LOW Voltage (Single−Ended)	V_{CCI} − 1.945		V_{CCI} − 1.6	V_{CCI} − 1.945		V_{CCI} − 1.6	V_{CCI} − 1.945		V_{CCI} − 1.6	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 2) (Figure 5) LVPECL_CLK/$\overline{\text{LVPECL\_CLK}}$	1.2		V_{CCI}	1.2		V_{CCI}	1.2		V_{CCI}	V
I_{IH}	Input HIGH Current	−150		150	−150		150	−150		150	μA
I_{IL}	Input LOW Current	−150		150	−150		150	−150		150	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. V_{IHCMR} max varies 1:1 with V_{CCI}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. LVTTL/LVCMOS DC CHARACTERISTICS V_{CCI} = 3.0 V to 3.6 V; V_{CCO} = 1.6 V to 2.0 V, GND = 0 V

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	Input HIGH Voltage	2.0			2.0			2.0			V
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V
I_{IH}	Input HIGH Current	−150		150	−150		150	−150		150	μA
I_{IL}	Input LOW Current	−300		300	−300		300	−300		300	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

Table 7. HSTL DC CHARACTERISTICS V_{CCI} = 3.0 V to 3.6 V; V_{CCO} = 1.6 V to 2.0 V, GND = 0 V

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OH}	Output HIGH Voltage (Note 3)	1.0		1.2	1.0		1.2	1.0		1.2	V
V_{OL}	Output LOW Voltage (Note 3)	0.1		0.4	0.1		0.4	0.1		0.4	V
V_{IH}	Input HIGH Voltage (Figure 6)	V_X + 0.1		1.6	V_X + 0.1		1.6	V_X + 0.1		1.6	V
V_{IL}	Input LOW Voltage (Figure 6)	−0.3		V_X − 0.1	−0.3		V_X − 0.1	−0.3		V_X − 0.1	V
V_X	HSTL Input Crossover Voltage	0.68	−	0.9	0.68	−	0.9	0.68	−	0.9	V
I_{IH}	Input HIGH Current	−150		150	−150		150	−150		150	μA
I_{IL}	Input LOW Current	−300		300	−300		300	−300		300	μA
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) HSTL_CLK/$\overline{\text{HSTL\_CLK}}$	0.6		V_{CCI} − 1.2	0.6		V_{CCI} − 1.2	0.6		V_{CCI} − 1.2	V V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. All outputs loaded with 50 Ω to GND (Figure 7).
4. V_{IHCMR} max varies 1:1 with V_{CCI}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. AC CHARACTERISTICS V_{CCI} = 3.0 V to 3.6 V; V_{CCO} = 1.6 V to 2.0 V, GND = 0 V (Note 5)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{Opp}	Differential Output Voltage (f_{out} < 100 MHz (Figure 4) f_{out} < 500 MHz f_{out} < 750 MHz	600 600 450	850 750 575		600 600 450	850 750 575		600 600 450	850 750 575		 mV mV
t_{PLH} t_{PHL}	Propagation Delay (Differential Configura- tion) LVPECL_CLK to Q HSTL_CLK to Q	 680 690	 800 830	 930 990	 700 700	 820 850	 950 1000	 780 790	 920 950	 1070 1110	 ps ps
t_{skew}	Within−Device Skew (Note 6) Device−to−Device Skew (Note 7)		15 100	50 200		15 100	50 200		15 100	50 200	ps ps
t_{JITTER}	Random Clock Jitter (Figure 4) (RMS)		1.4	3.0		1.4	3.0		1.4	3.0	ps
V_{PP}	Input Swing (Differential Configuration) (Note 8) (Figure 5) LVPECL HSTL	 200 200			 200 200			 200 200			 mV mV
t_S	OE Set Up Time (Note 9)	0.5			0.5			0.5			ns
t_H	OE Hold Time	0.5			0.5			0.5			ns
t_r/t_f	Output Rise/Fall Time (20% − 80%)	350		600	350	450	600	350		600	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Measured with 750 mV (LVPECL) source or 1 V (HSTL) source, 50% duty cycle clock source. All outputs loaded with 50 Ω to GND (Figure 7).
6. Skew is measured between outputs under identical transitions and conditions on any one device.
7. Device−to−Device skew for identical transitions and conditions.
8. V_{PP} is the Differential Input Voltage swing required to maintain AC characteristics listed herein.
9. OE Set Up Time is defined with respect to the rising edge of the clock. OE High−to−Low transition ensures outputs remain disabled during the next clock cycle. OE Low−to−High transition enables normal operation of the next input clock (Figure 9).

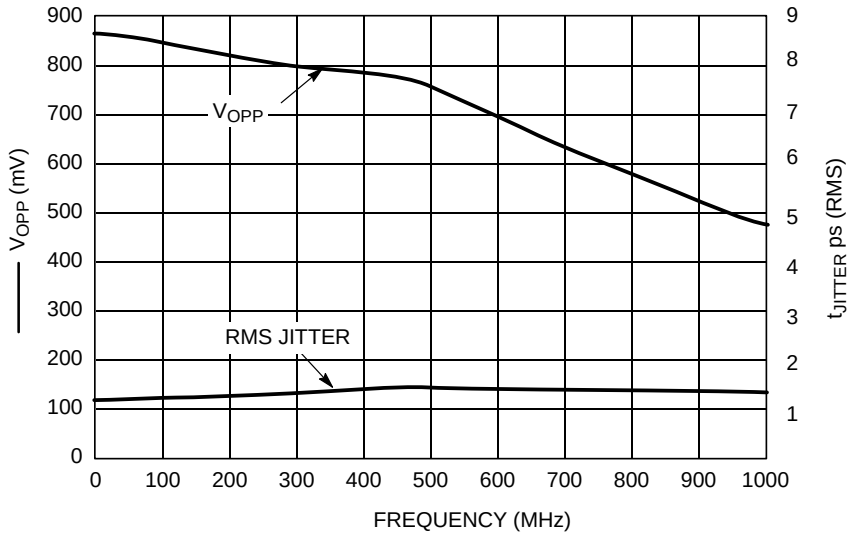


Figure 4. Output Frequency (F_{OUT}) versus Output Voltage (V_{OPP}) and Random Clock Jitter (t_{JITTER})

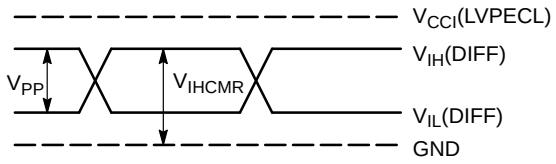


Figure 5. LVPECL Differential Input Levels

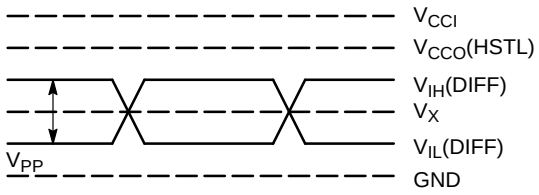


Figure 6. HSTL Differential Input Levels

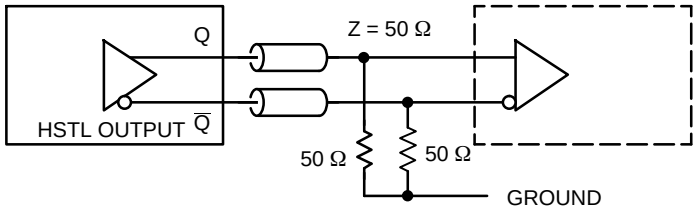
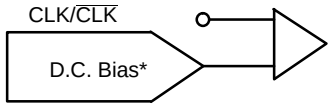


Figure 7. HSTL Output Termination and AC Test Reference



*Must be CLK/$\overline{CLK}$ common mode voltage: $((V_{IH} + V_{IL})/2)$.

Figure 8. Single−Ended CLK/$\overline{CLK}$ Input Configuration

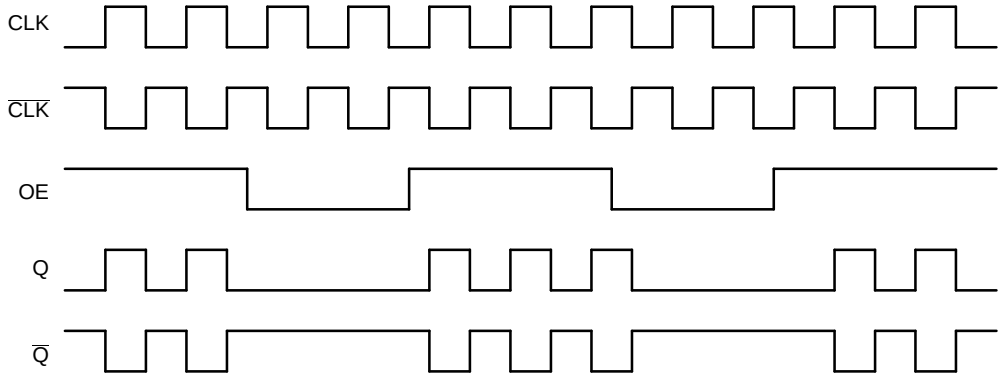


Figure 9. Output Enable (OE) Timing Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC100EP809FAG	LQFP−32 (Pb−Free)	250 Units / Tray
MC100EP809FAR2G	LQFP−32 (Pb−Free)	2000 / Tape & Reel
MC100EP809MNG	QFN32 (Pb−Free)	74 Units / Rail
MC100EP809MNR4G	QFN32 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1672/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

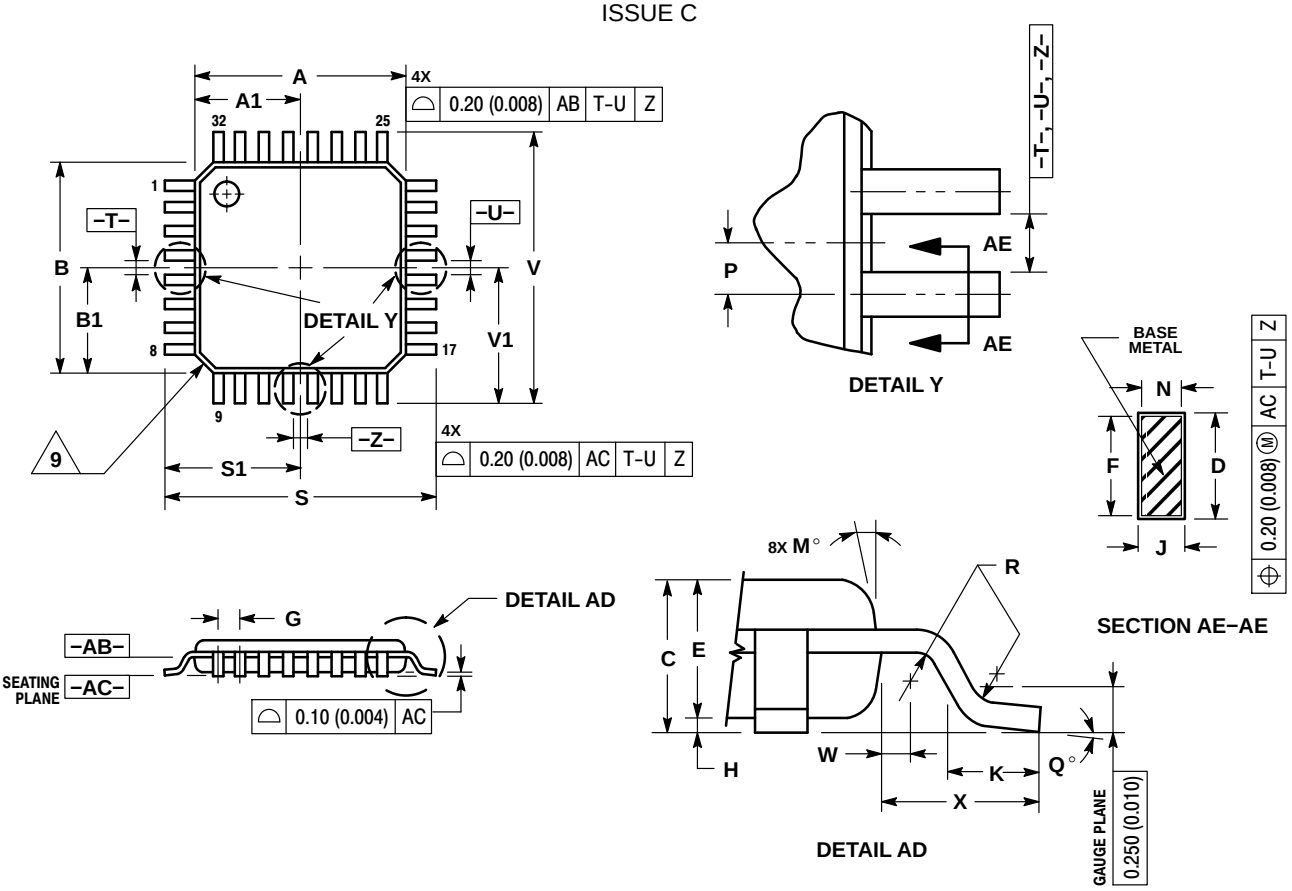
AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

32 LEAD LQFP
CASE 873A−02
ISSUE C

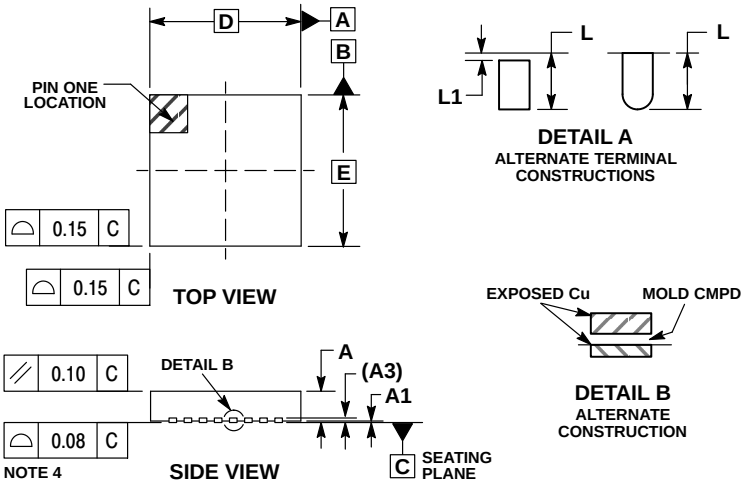


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −AB− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS −T−, −U−, AND −Z− TO BE DETERMINED AT DATUM PLANE −AB−.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE −AC−.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −AB−.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.750	0.018	0.030
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

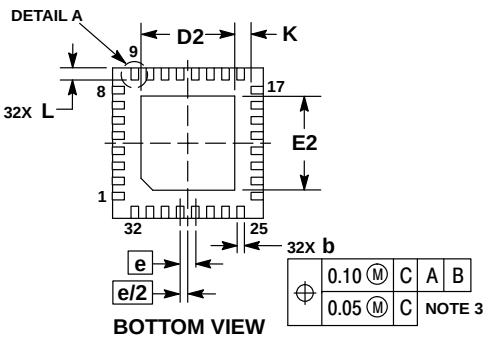
PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

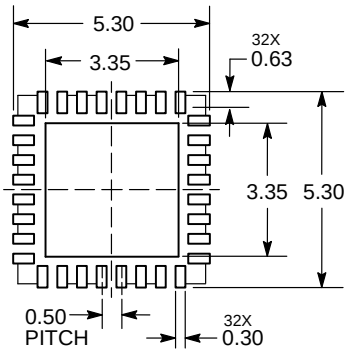


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	−−−	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50
L1	−−−	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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Japan Customer Focus Center
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ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative